

REMARKS

The Official Action mailed July 24, 2007, has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time. Accordingly, the Applicant respectfully submits that this response is being timely filed.

The Applicant notes with appreciation the consideration of the Information Disclosure Statement filed on March 18, 2007.

A further Information Disclosure Statement is submitted herewith and consideration of this Information Disclosure Statement is respectfully requested.

Claims 1-25 were pending in the present application prior to the above amendment. Claims 2-5, 8, 9, 12, 13 and 15-22 have been withdrawn from consideration by the Examiner (page 3, Paper No. 20070720). Claims 1, 7, 11 and 23-25 have been amended to better recite the features of the present invention, and new dependent claims 26-31 have been added to recite additional protection to which the Applicant is entitled. Accordingly, claims 1, 6, 7, 10, 11, 14 and 23-31 are currently elected, of which claims 1, 6, 7 and 23-25 are independent. For the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

Paragraph 7 of the Official Action rejects claims 1, 6, 7, 10, 11, 14 and 23-25 as anticipated by U.S. Patent No. 6,774,877 to Nishitoba. The Applicant respectfully submits that an anticipation rejection cannot be maintained against the independent claims of the present application.

As stated in MPEP § 2131, to establish an anticipation rejection, each and every element as set forth in the claim must be described either expressly or inherently in a single prior art reference. Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

The Applicant respectfully submits that an anticipation rejection cannot be maintained against the independent claims of the present application. Specifically,

claims 1, 7, 11 and 23-25 recite that a channel length of a first transistor is longer than a channel width thereof. For the reasons provided below, the Applicant respectfully submits that Nishitoba does not teach the above-referenced features of the present invention, either explicitly or inherently.

The Official Action asserts that Nishitoba discloses "two transistors (ref. #8 and #9)" and "varying the channel length of transistor (ref. #9) with respect to the channel length of the transistor (ref. #8)(see e.g. col. 6, lines 38-59; col. 7, lines 23-57; figs. 5 and 6), which imply that the size of the transistor's channel, i.e. length and width, would be a choice of experimental design and is considered within the purview of the cited prior art" (page 4, Paper No. 20070720). The Applicant respectfully disagrees and traverses the assertions in the Official Action.

The transistor 9 of Nishitoba is connected to the light emitting element through the transistor 8. Therefore, it might be argued that the transistors 8 and 9 correspond to the first transistor and the second transistor of the subject application, respectively. However, Nishitoba discloses that the channel length of the transistor 8 is 4 mm, that the channel width of the transistor 8 is 4 mm, that the channel width of the transistor 9 is 4 mm, that the channel length of the transistor 9 is preferably set to at least 0.5 times the channel length of transistor 8, and more preferably to at least one time but not greater than four times the channel length of the transistor 8 (column 7, lines 39-58).

Thus, Nishitoba discloses that the channel length of the transistor 9 (allegedly corresponding to the second transistor of the claimed invention) is equal to the channel width of the transistor 9 and that the channel length of the transistor 8 (allegedly corresponding to the first transistor of the claimed invention) is equal to the channel width of the first transistor 8. However, Nishitoba appears to fail to disclose that the channel length of the first transistor is longer than the channel width of the first transistor. Also, Nishitoba does not teach, either explicitly or inherently, that the ratio of the channel length to the channel width should be modified, much less that the channel length should be made longer than the channel width.

As noted above, the Official Action asserts that "the size of the transistor's channel, i.e. length and width, would be a choice of experimental design and is considered within the purview of the cited prior art" (page 4, Id.). For at least the reasons noted below, the Applicant respectfully disagrees and traverses the assertions in the Official Action.

In the present invention, the size of the first transistor, i.e. the channel length and the channel width, is set such that the first transistor operates in a saturation region. In the case where a first transistor operates in a saturation region, the drain current I_{d1} of the first transistor is calculated, for example, according to the formula "numeral 1" (page 8 of the present specification):

$$I_{d1} = \beta \cdot (V_{gs} - V_{th})^2 / 2$$

In the "numeral 1" formula, $\beta = \mu C_o W/L$, where μ indicates a mobility, C_o indicates a gate capacitance per unit area, and W/L indicates a ratio of the channel width W to the channel length L of the channel forming region (see paragraphs [0019] and [0020] of the present specification, pages 7-8). Therefore, in the case where a ratio of L/W increases, i.e., L (the channel length of the first transistor) increases, $(V_{gs} - V_{th})$ should increase in order to keep I_{d1} constant because β decreases, for example. Here, V_{th} is a specific value of each transistor (the first transistor in this case), so V_{gs} increases. Thus, a comparative influence of the variation of the threshold voltage to $V_{gs} - V_{th}$ increases. Therefore, the variation of the ON current due to the variation of the threshold voltage or the like can be suppressed.

In other words, varying the ratio of channel width to channel length has numerous potential effects on the overall function of the device. The disclosure at column 6, lines 38-59, and at column 7, lines 23-57 in Nishitoba does not discuss these effects at all and does not appear to be concerned with the ratio of length to width. Therefore, despite the general assertion in the Official Action, it is not at all clear that Nishitoba implies that the size or ratio of a transistor's channel, i.e. length and width, would be a choice of experimental design. The Applicant respectfully submits that one

of ordinary skill in the art at the time of the present invention, upon reviewing Nishitoba, would not necessarily modify the ratio of the channel length and the channel width as a mere choice of experimental design, and would not necessarily modify the ratio such that a channel length of a first transistor is longer than a channel width thereof.

Therefore, the Applicant respectfully submits that Nishitoba does not teach that a channel length of a first transistor is longer than a channel width thereof, either explicitly or inherently.

Since Nishitoba does not teach all the elements of the independent claims, either explicitly or inherently, an anticipation rejection cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 102 are in order and respectfully requested.

Paragraph 8 of the Official Action rejects claims 1, 6, 7, 10, 23 and 24 as anticipated by EP 1 310 997 to Udagawa. The Applicant respectfully submits that an anticipation rejection cannot be maintained against the independent claims of the present application, as amended.

Independent claims 1, 7, 11 and 23-25 have been amended to recite that a first electrode of a first transistor is connected to a light emitting element and that a second electrode of the first transistor is connected to a second transistor. Also, independent claims 1 and 7 recite that a threshold voltage of a first transistor is higher than a threshold voltage of a second transistor and claim 11 recites that a threshold of a first transistor is higher than a threshold of a second transistor. For the reasons provided below, the Applicant respectfully submits that Udagawa does not teach the above-referenced features of the present invention, either explicitly or inherently.

The Official Action asserts that Udagawa discloses that "two transistors (ref. #701) ... [are] connected to the organic EL element in a series (see e.g. section [0135]) ... [and] the threshold voltage of the transistor is dependent on its channel length (see e.g. sections: [0016], [0018], [0019] and [0021]-[0025])" (page 5, Paper No. 20070720).

However, the Applicant respectfully submits that the amended independent claims are distinguishable over Udagawa. As mentioned above, claims 1, 7, 11 and 23-25 have been amended to recite that a first electrode of a first transistor is connected to a light emitting element and that a second electrode of the first transistor is connected to a second transistor. Although one of the transistors 701 of Udagawa is connected to the gate electrode of the transistor 702, neither of the transistors 701, 702 is connected to the light emitting element in the manner claimed, i.e. such that a first electrode of a first transistor is connected to a light emitting element and such that a second electrode of the first transistor is connected to a second transistor. Therefore, the Applicant respectfully submits that Udagawa does not teach that a first electrode of a first transistor is connected to a light emitting element and that a second electrode of the first transistor is connected to a second transistor, either explicitly or inherently.

Also, with respect to claims 1, 7 and 11, as noted above, the Official Action asserts that Udagawa discloses that "the threshold voltage of the transistor is dependent on its channel length (see e.g. sections: [0016], [0018], [0019] and [0021]-[0025])" (page 5, Paper No. 20070720). However, in these sections, Udagawa appears to describe a gate voltage value and does not appear to mention a relationship between a threshold voltage and characteristics of a transistor. Therefore, the Applicant respectfully submits that Udagawa does not disclose that a threshold (voltage) of a first transistor is higher than a threshold (voltage) of a second transistor, either explicitly or inherently.

Since Udagawa does not teach all the elements of the independent claims, either explicitly or inherently, an anticipation rejection cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 102 are in order and respectfully requested.


Paragraph 11 of the Official Action rejects claims 23 and 24 under the doctrine of obviousness-type double patenting over claims 3, 4, 7, 8, 11, 12, 15 and 16 of U.S. Application Serial No. 11/208,278 (U.S. Publication No. 2006/0044229) to Yamazaki.

Paragraph 12 of the Official Action rejects claims 23 and 24 under the doctrine of obviousness-type double patenting over claims 1, 2, 6, 7, 11 and 12 of U.S. Application Serial No. 11/565,116 (U.S. Publication No. 2007/0126666) to Yamazaki. In response, the Applicant respectfully requests that the double patenting rejections be held in abeyance until an indication of allowable subject matter is made in either the present application or the copending applications. At such time, the Applicant will respond to any remaining double patenting rejections.

New dependent claims 26-31 have been added to recite additional protection to which the Applicant is entitled. For the reasons stated above and already of record, the Applicant respectfully submits that new claims 26-31 are in condition for allowance.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,



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